Section III: Recoverable SEU Effects

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SEE Effects in Operational Spacecraft

"Safehold" Condition in DS-1 Shortly after Launch

Multiple-Bit Errors in Cassini Solid-State Recorder

- Occurred even though extensive testing was done during design phase
- Attributed to system architectural flaw

Inadvertent Switching of Cassini Power Modules to Standby Mode

- Caused by transients from PM139 comparator
- Low probability because of high input voltage used in design

Single-Event Upset

First Observed in Bipolar Flip-Flops in 1979

- Original work treated with skepticism
- SEU has emerged as one of the major issues for application of microelectronics in space

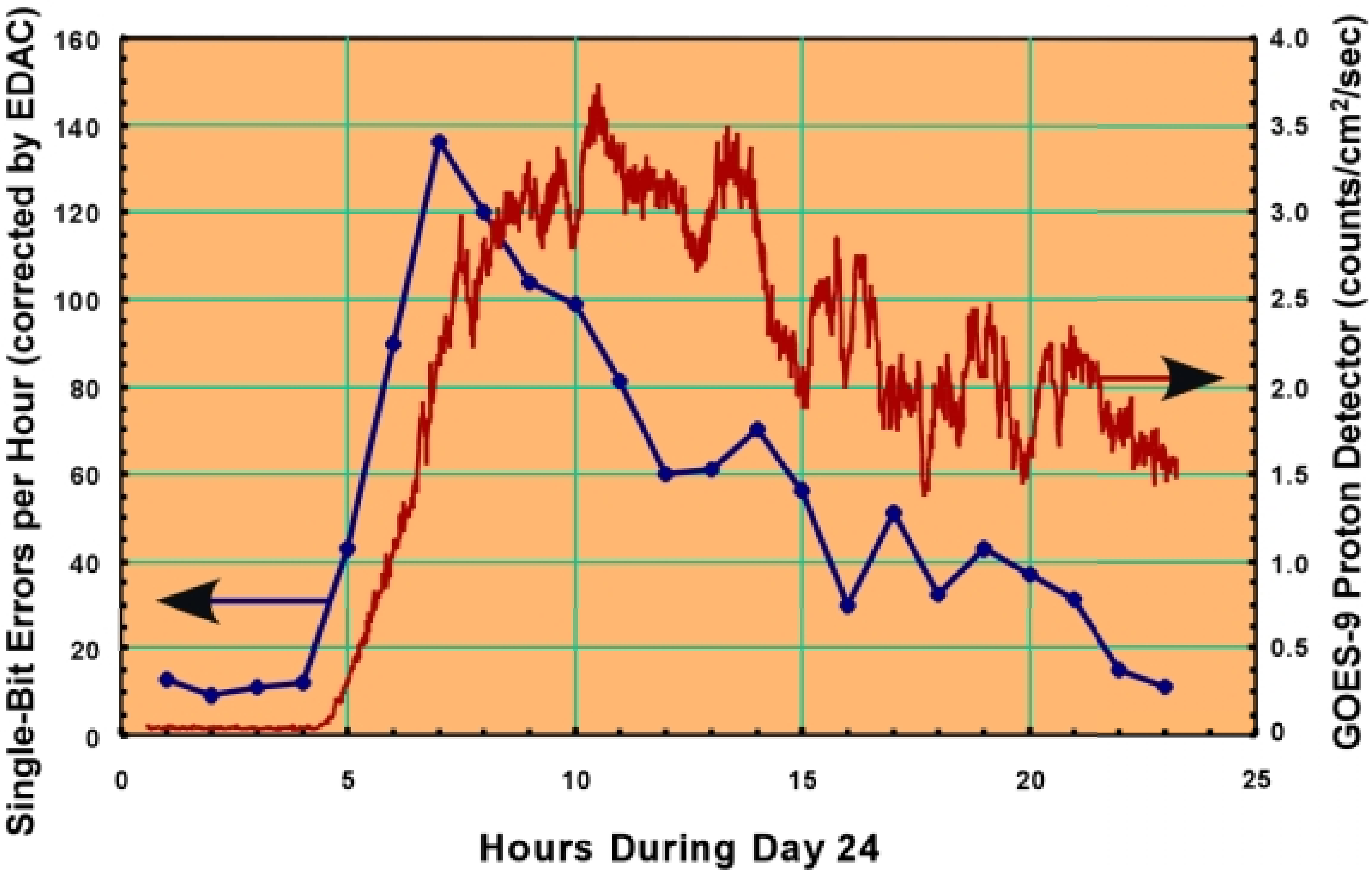
Previous JPL Missions Have Struggled with SEU Problems

- Galileo used a 2901 bit-slice microprocessor (bipolar technology)
- Initial testing showed SEU susceptibility, at moderate rate
- Subsequent die design changes increased the SEU rate beyond the point where the device was useable
- Sandia National Laboratory designed a special rad-hard CMOS version that was used on the spacecraft

SEU Effects Have Become Worse as Devices Have Evolved

- Lower “critical charge” because of small device dimensions
- Large numbers of transistors per chip and overall complexity

Cassini SSR Errors During Solar Flare



Overview

How storage elements are upset

- SRAM
- DRAM

What are “cross-section” and “L.E.T.”

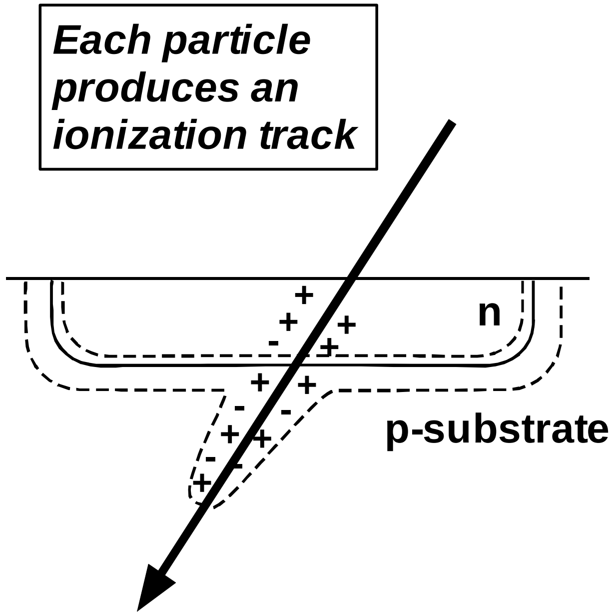
How space upset rates are calculated

Upset mitigation techniques

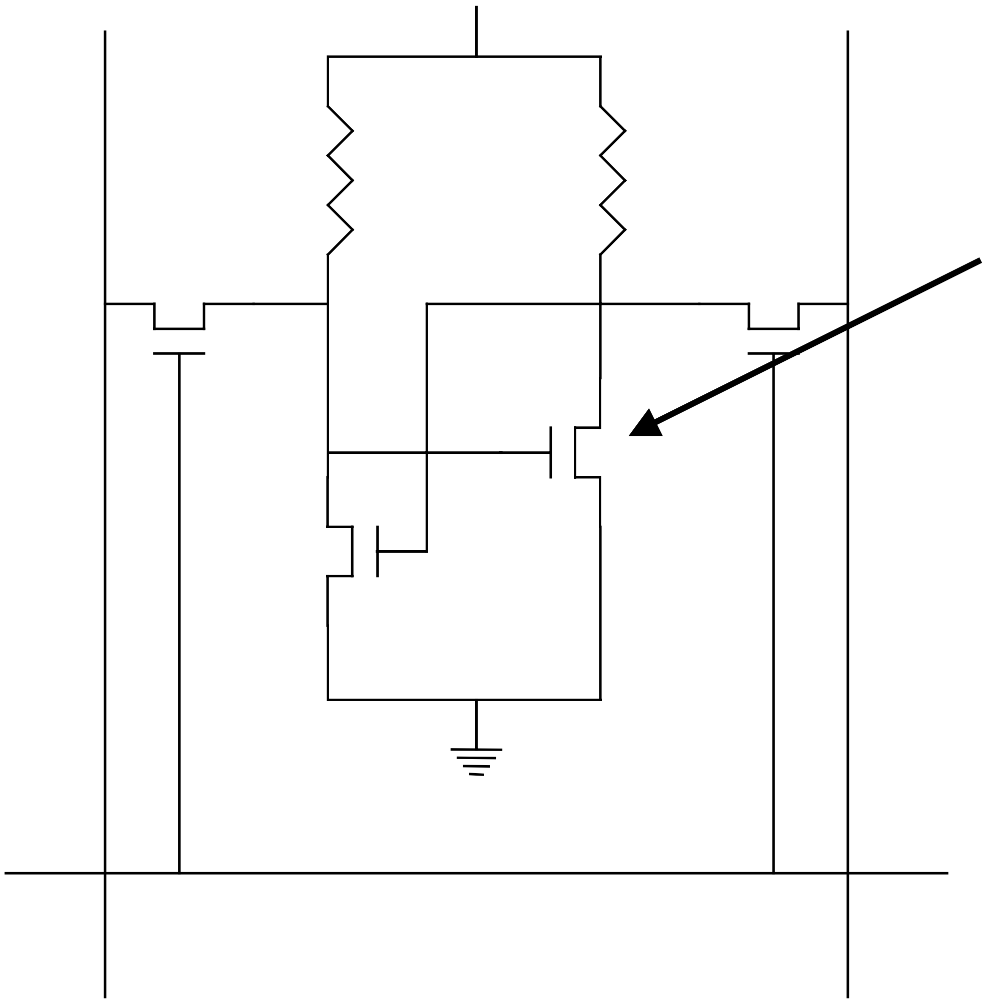
Other effects

- SEFI
- Transients

Ion Strike on a p-n Junction



How an SRAM Cell Upsets



Ion strike on or near transistor will change bit state

What is LET?

Measure of energy deposition in a material

- for example: silicon

Linear Energy Transfer

Units are MeV per mg/cm^2 (energy per areal density)

Proportional to MeV/μ or pC/μ

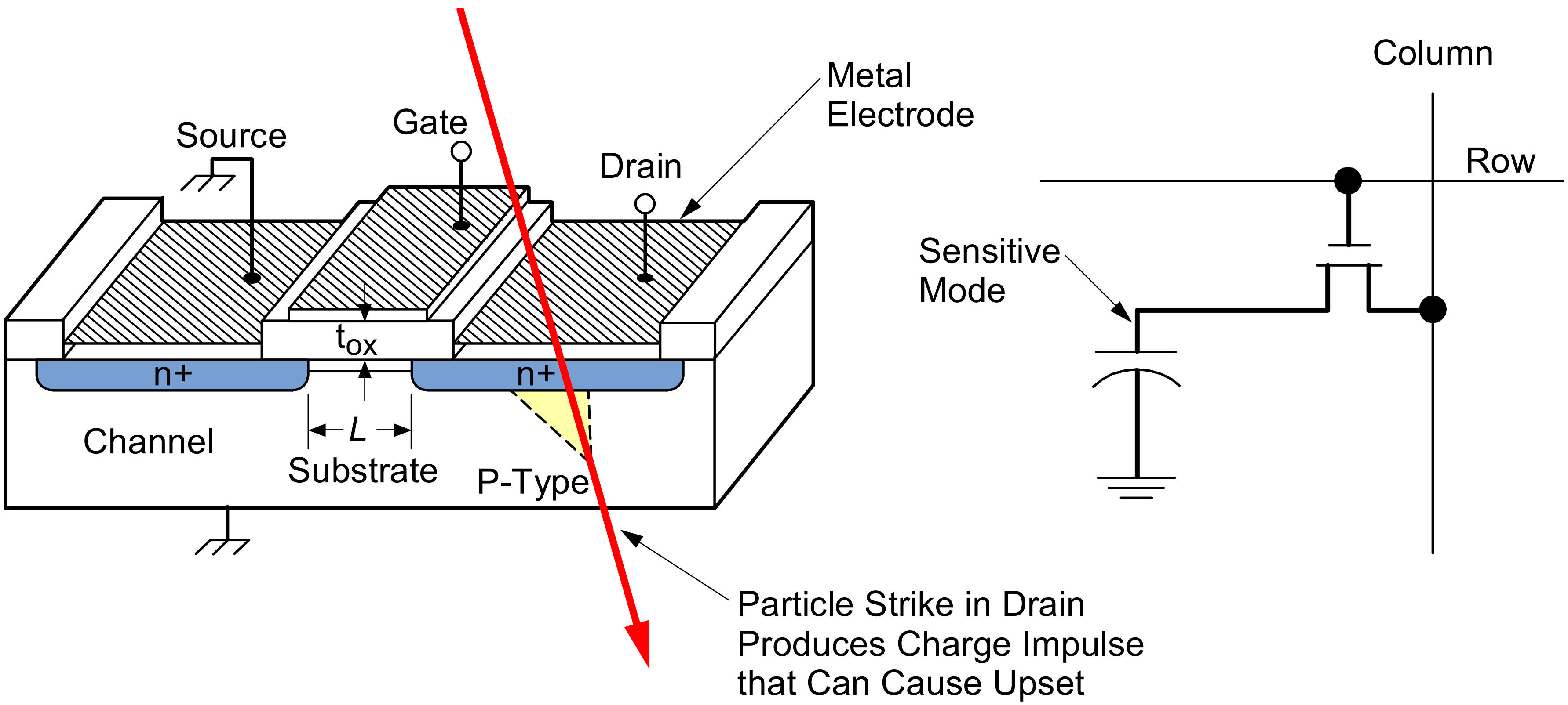
What is Cross Section?

Measure Of Susceptibility

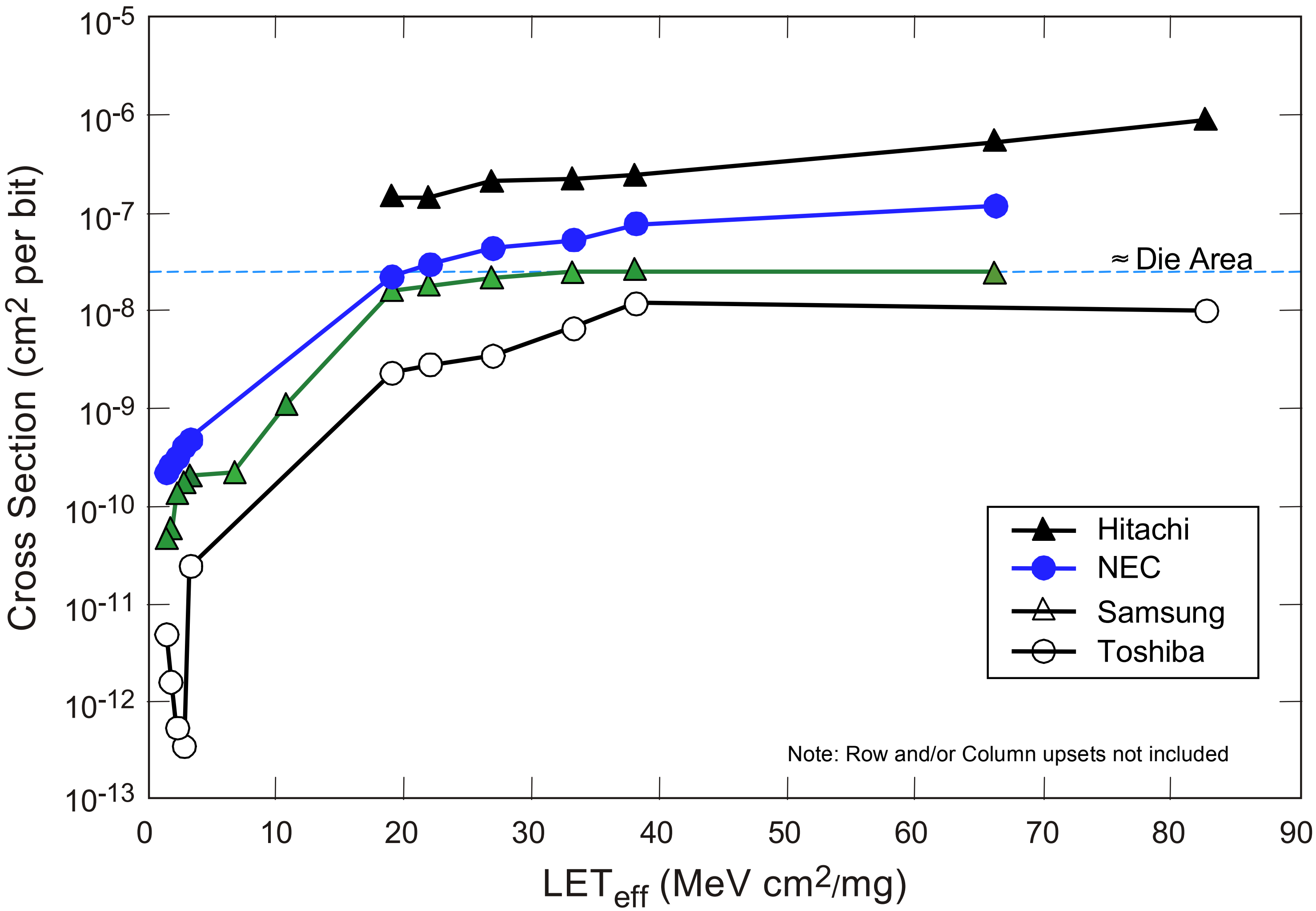
Units = area (cm^2 or μ^2)

Dart Board Analogy

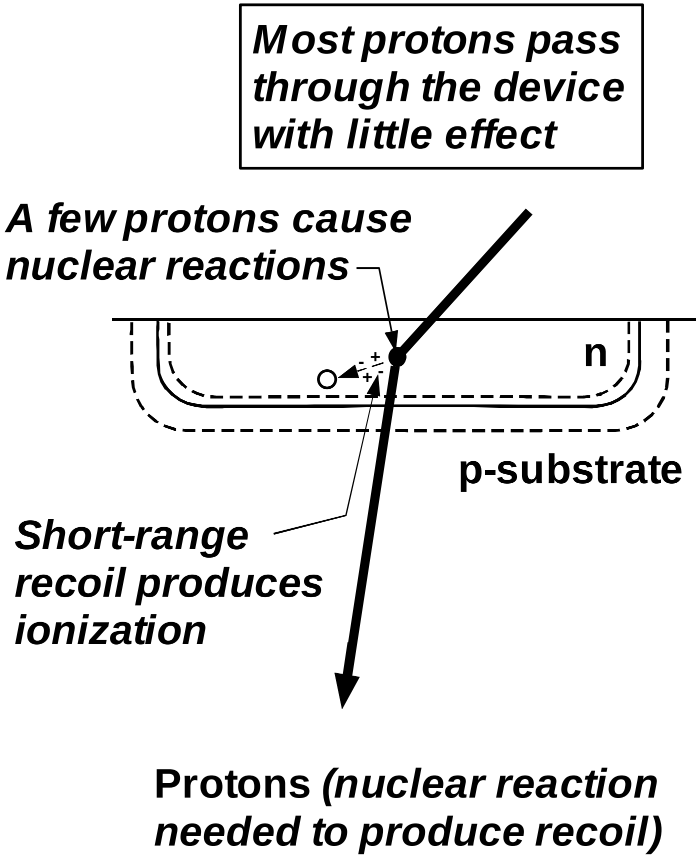
Upset Mechanism for DRAMs



Single-Event Upset in 64-Mb DRAMs



Proton Reaction in a p-n Junction



Upset from Protons

Proton LET Is Extremely Low

- Proton upset is usually dominated by nuclear reactions
- Secondary reaction products have much higher LET, but have short ranges compared to galactic cosmic rays

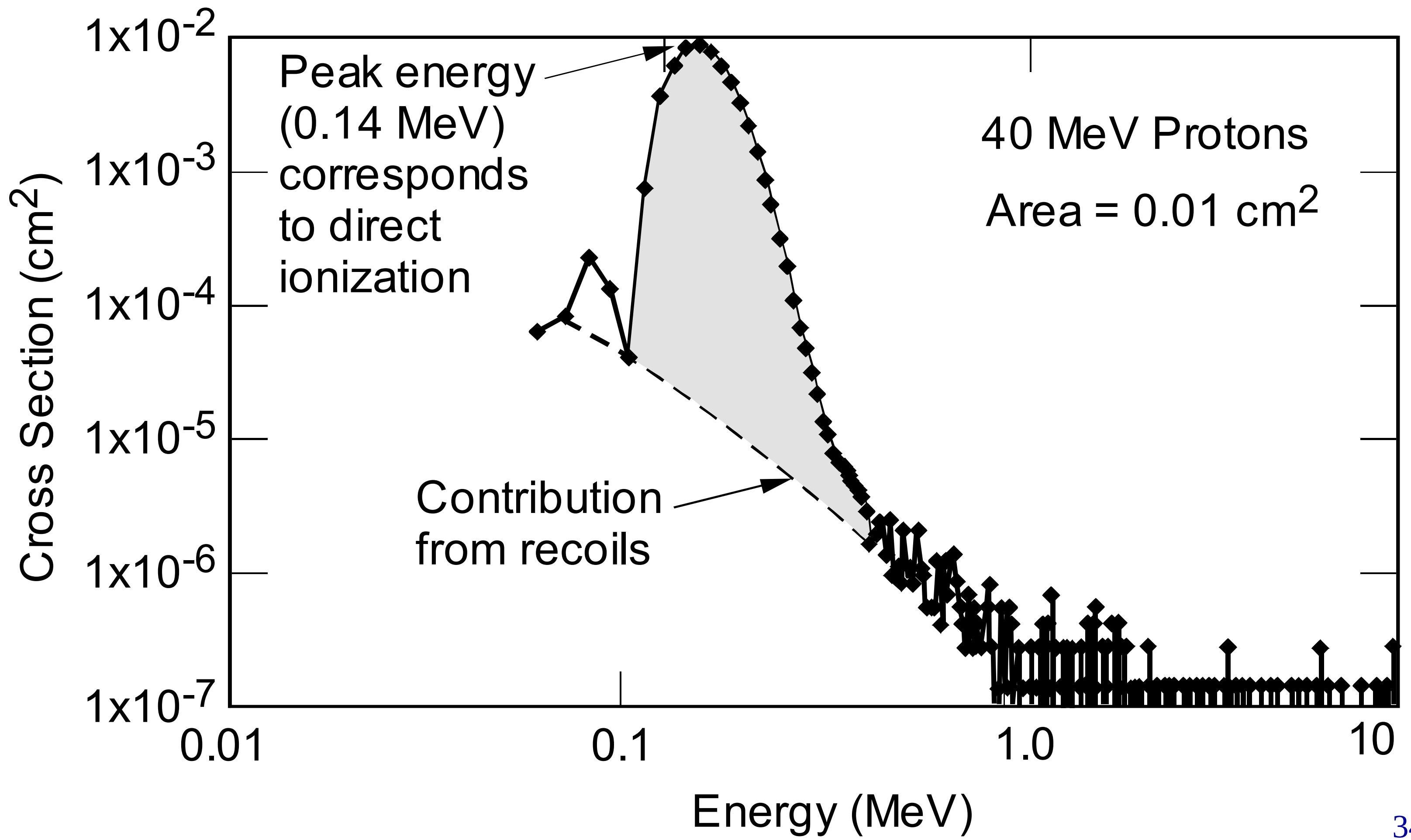
Proton Testing Provides only Limited Information about SEE Sensitivity

- "Effective" LET of protons is 3-12 MeV-cm^2/mg
- Depends on device construction

Significance of Proton Upset

- Important because protons can make a large contribution to the overall upset rate (particularly for low earth orbits)
- Proton testing is cheaper and easier than tests with heavy ions
- In many cases proton test data may be the only available information

Proton Recoil Distribution in a Surface Barrier Detector that Is 50 µm Thick



How Space Upset Rates Are Calculated

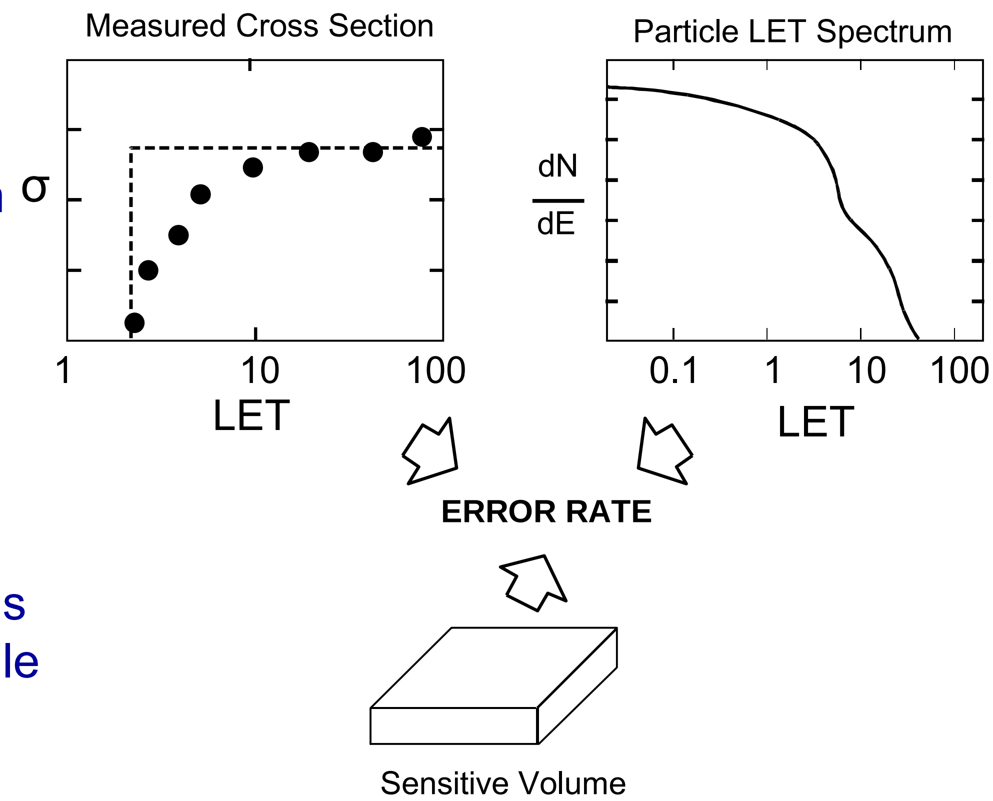
Measure σ vs. LET

- Testing done at high-energy accelerator
- Cross-section determined from circuit response

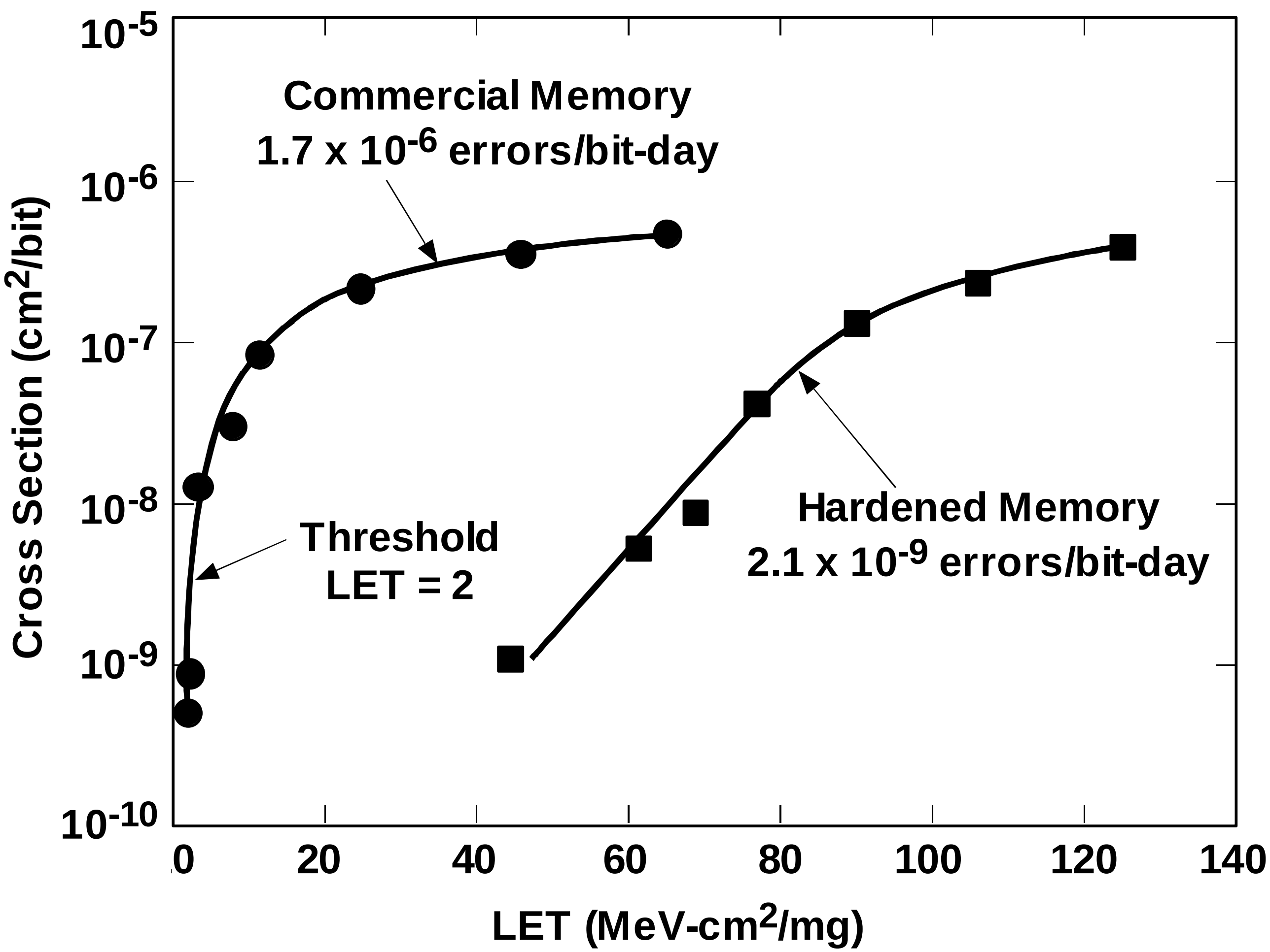
Determine Sensitive Volume

- Requires assumptions about device construction
- Used to determine effect of ions that strike the device at an angle

Integrate with LET Spectrum

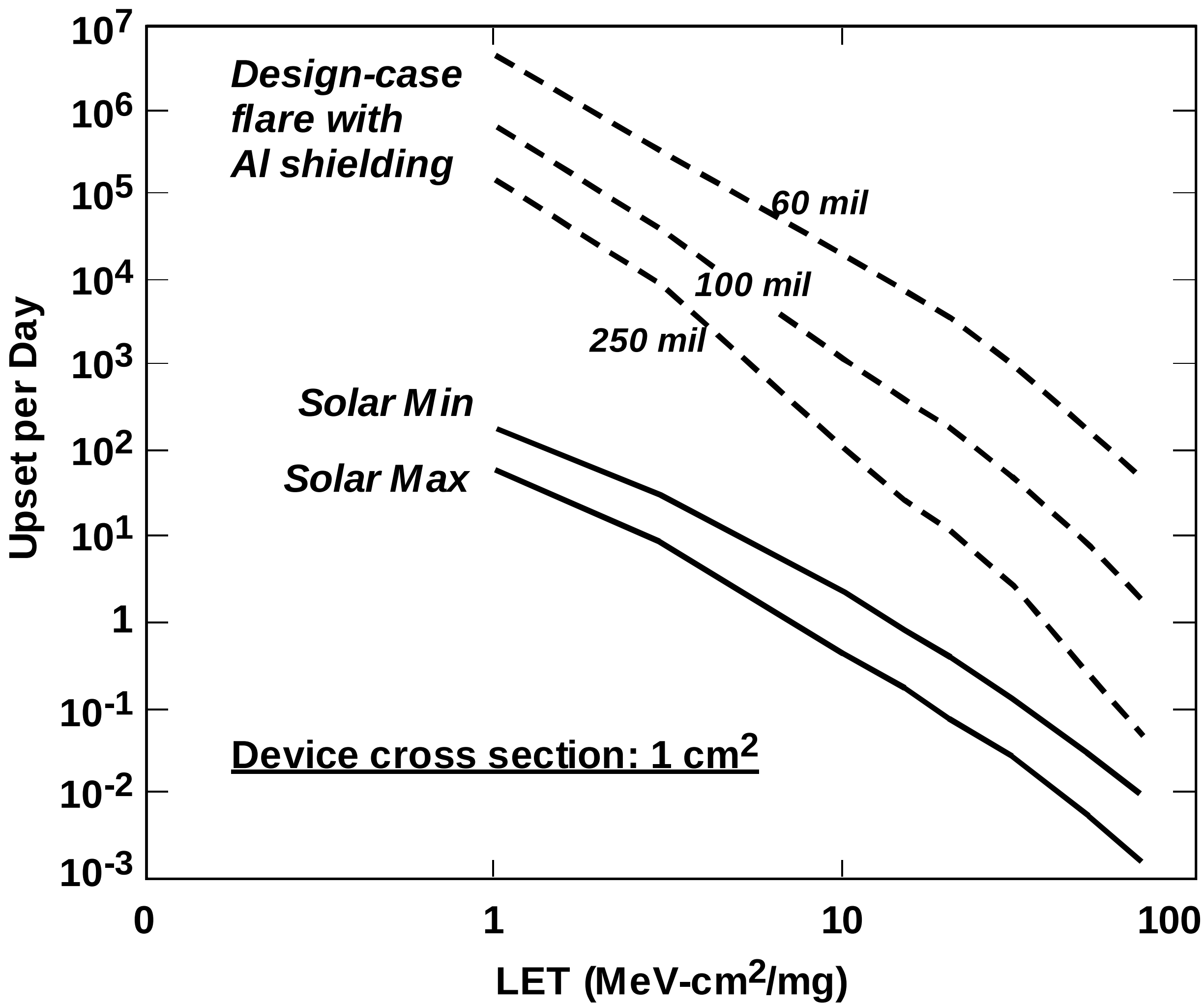


Dependence of Cross Section on Stopping Power

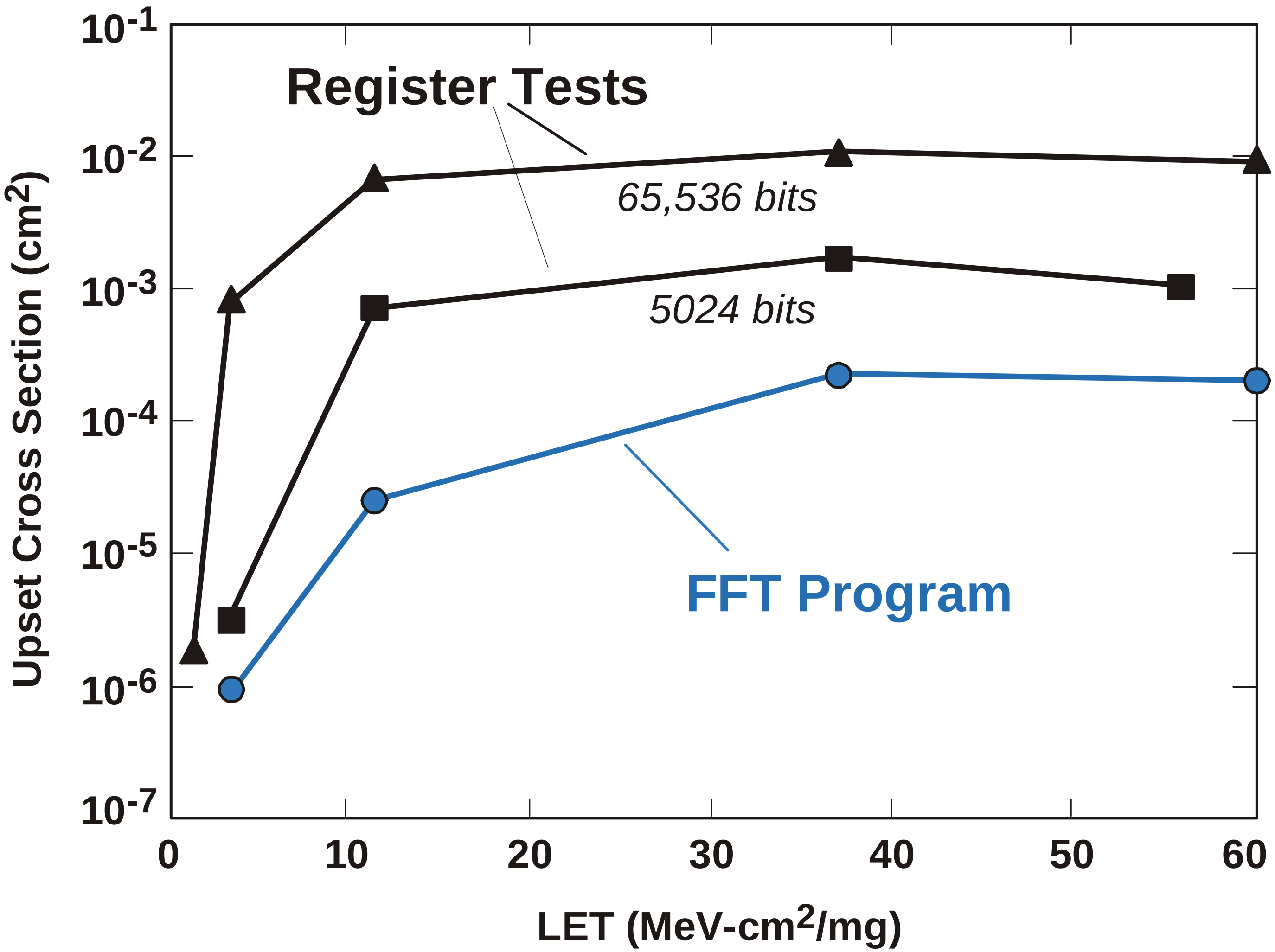


SEU Rates

(Interplanetary Space)



Dependence of PC603e Cross Section on Test Method



Hamming Codes

“SECDED” = Single Error Correction
Double error Detection
- example: (39, 32) = 32 data bits + 7 parity

“DECTED” = Double Error Correction
Triple Error Detection
- example: (79, 64) = 64 data bits + 15 parity

EDAC word error rate is approximately one half of:

$$\frac{T_{scrub}}{N_{EDAC}} \quad U^2$$

EDAC Issues

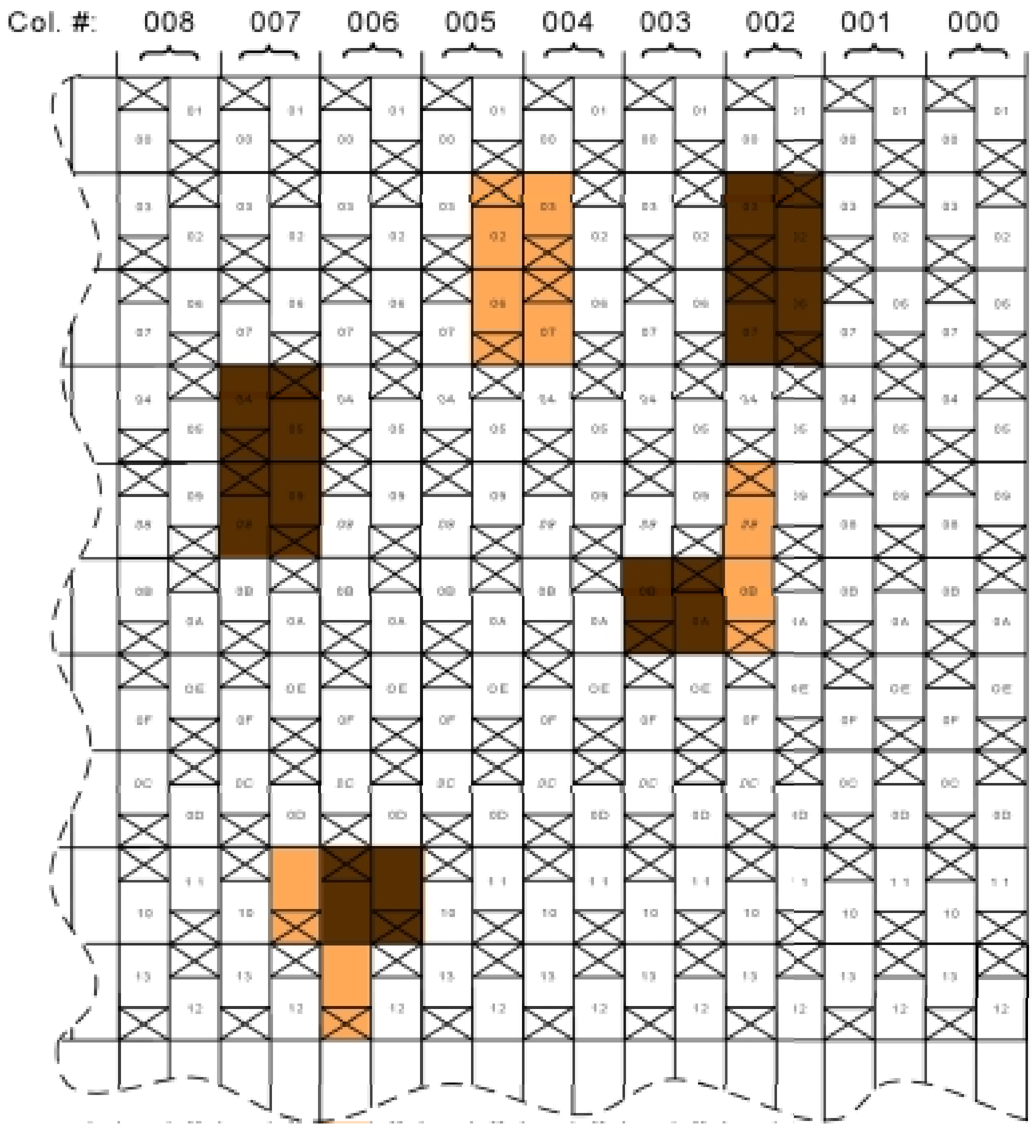
Error-detection-and-correction

- Used in solid-state recorders on many JPL spacecraft
- Different levels of correction, depending on algorithm
  - Single and double bit detection, with single-bit correction
  - Double bit detection and correction (larger word size)

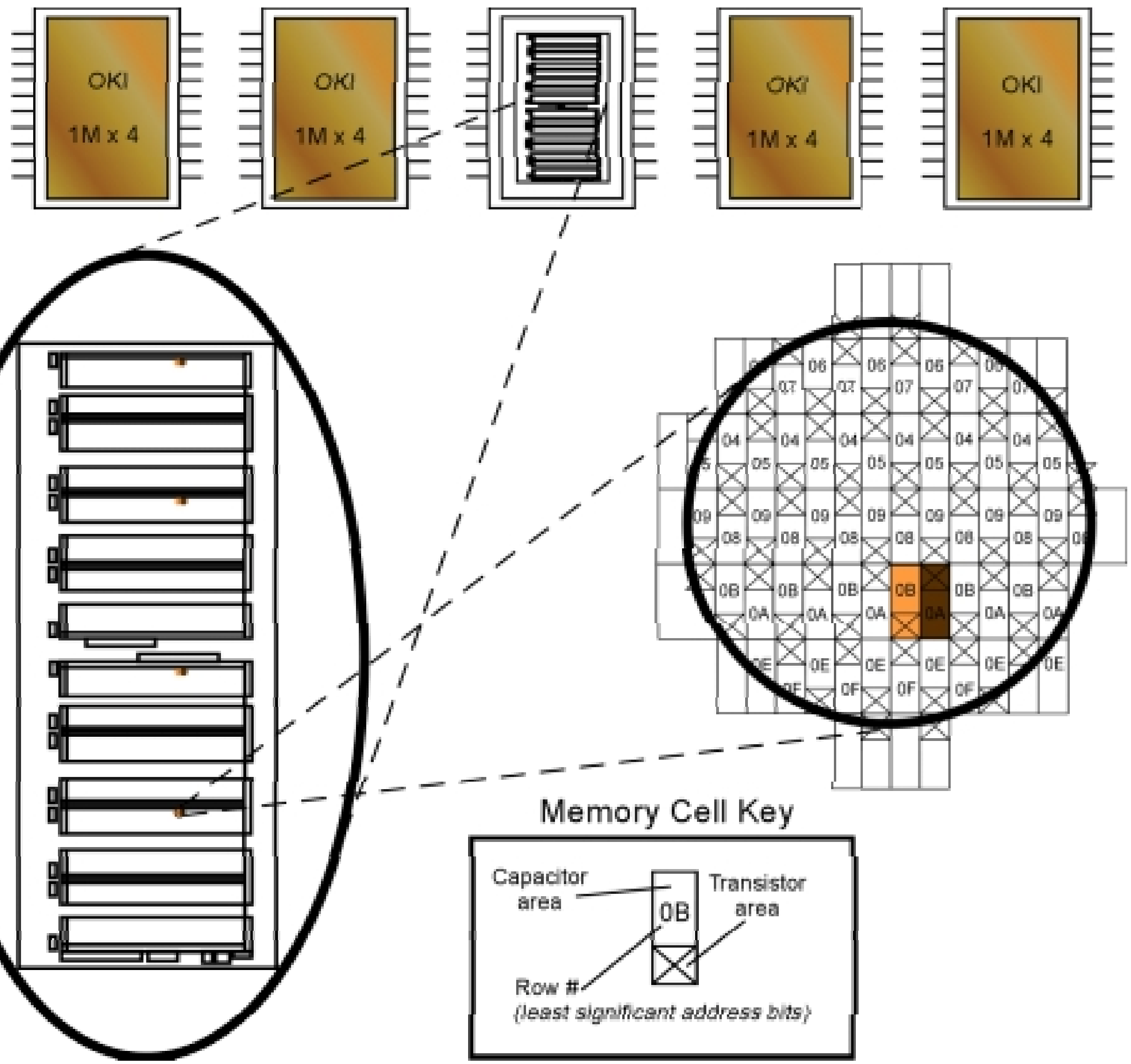
EDAC algorithms can fail at high rates

- Solar flares
- Transitions through radiation belts

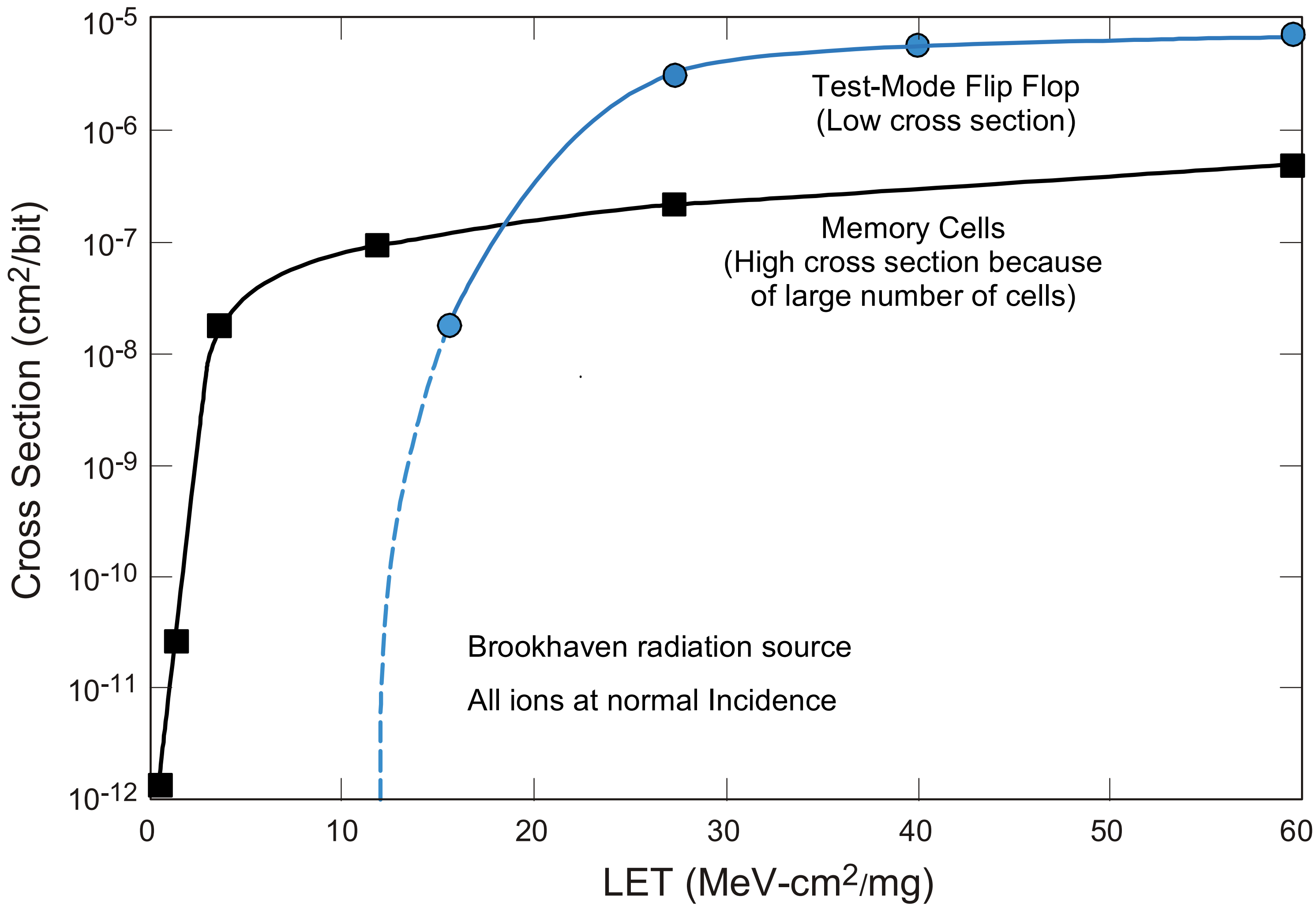
Multiple Bit Upsets in OKI DRAM



Cassini SSR Architectural Flaw



Functional Interrupt Effect ("SEFI")



Circuit Technologies where SEFI Is Important

Advanced Memories

- Internal test modes
- Microprogrammed cell architecture

Flash Memories

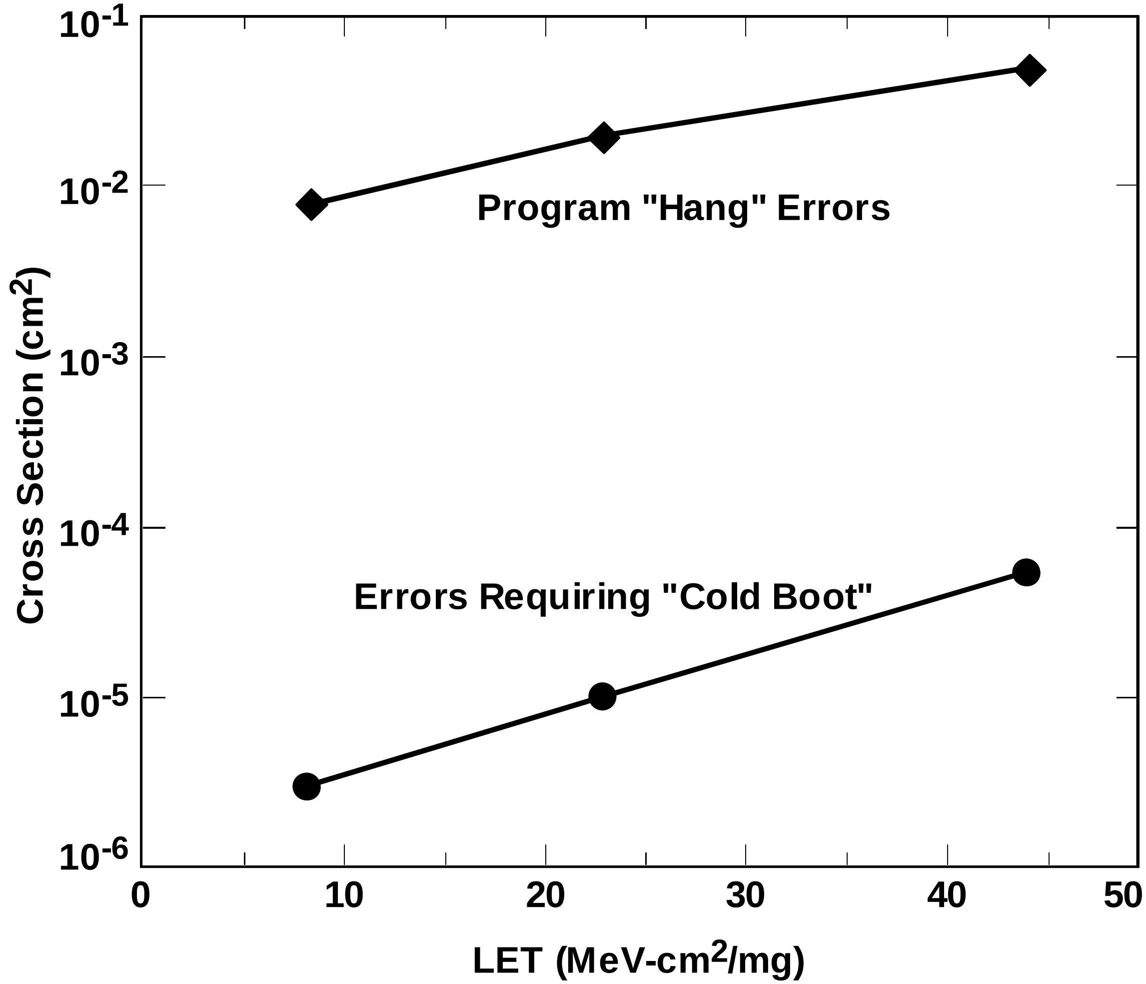
- Dominant effect
- “Crashes” internal state controller and buffers

Xilinx Programmable Logic Arrays

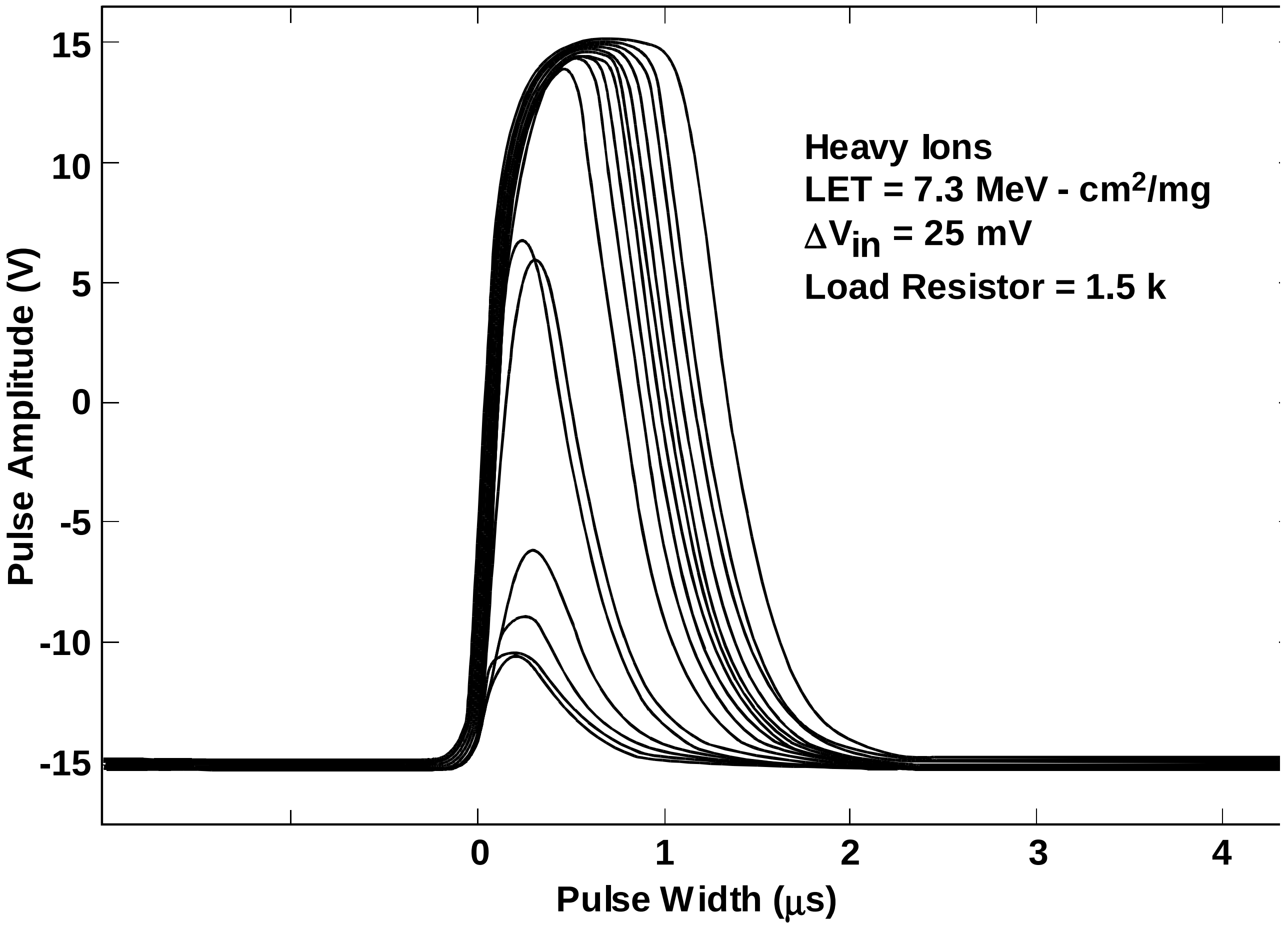
Microprocessors

- Many categories of responses
- Detection and recovery are very difficult problems

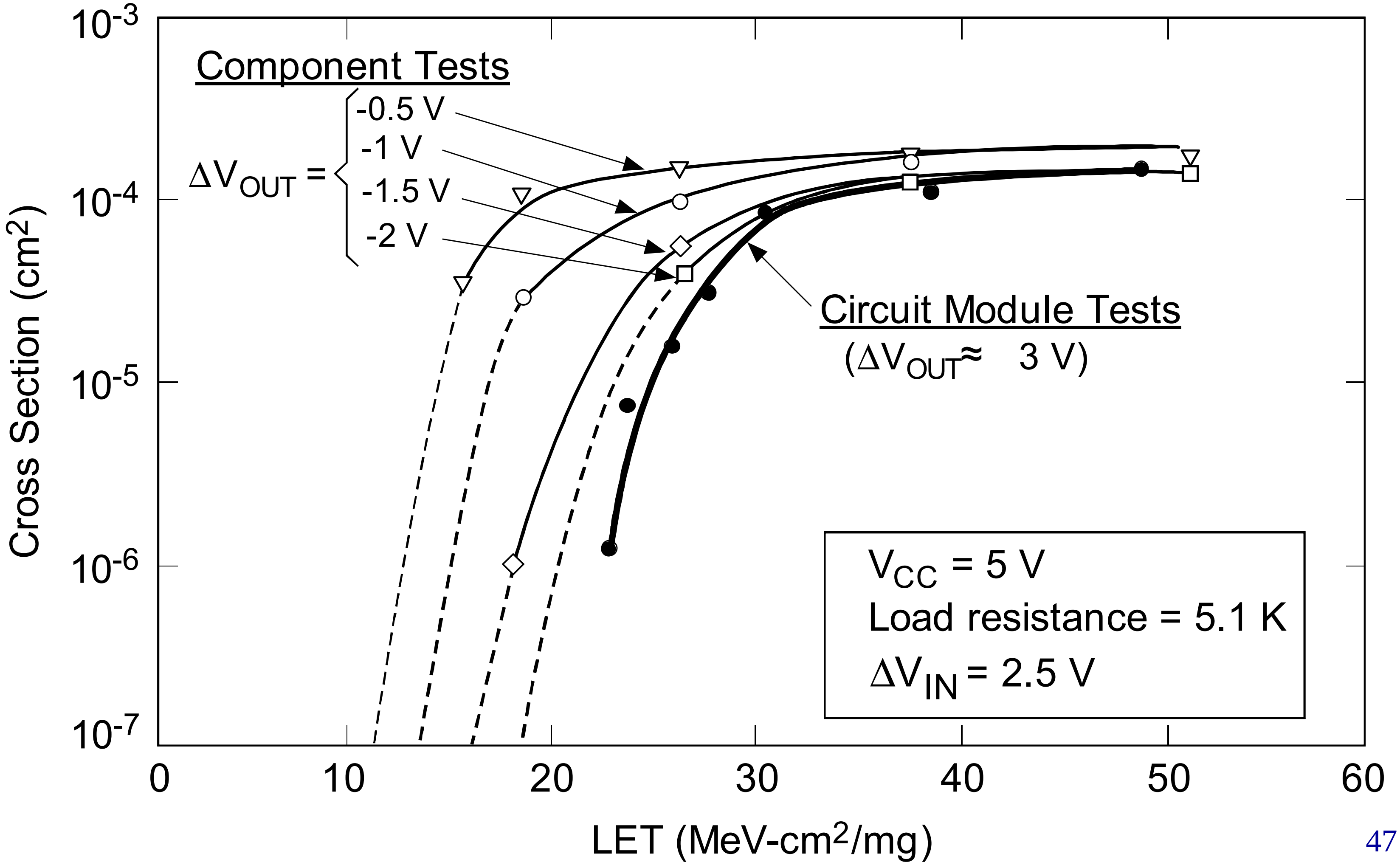
Non-Recoverable Errors in the 486 Processor



Output Pulses from Ion Strikes on a Comparator



Cross Section for Transients in the PM139 Comparator



Calculated Upset Rate for Cassini Power Modules

Assumed Environment	Aspect Ratio	Errors per Switch-Day
GCR, solar minimum	5:1	4.5×10^{-5}
GCR, solar maximum	5:1	8.2×10^{-6}
Design-case solar flare	5:1	1.6×10^{-2}

SEE Testing

Why so expensive?

Remote, Expensive Facilities (Accelerators)

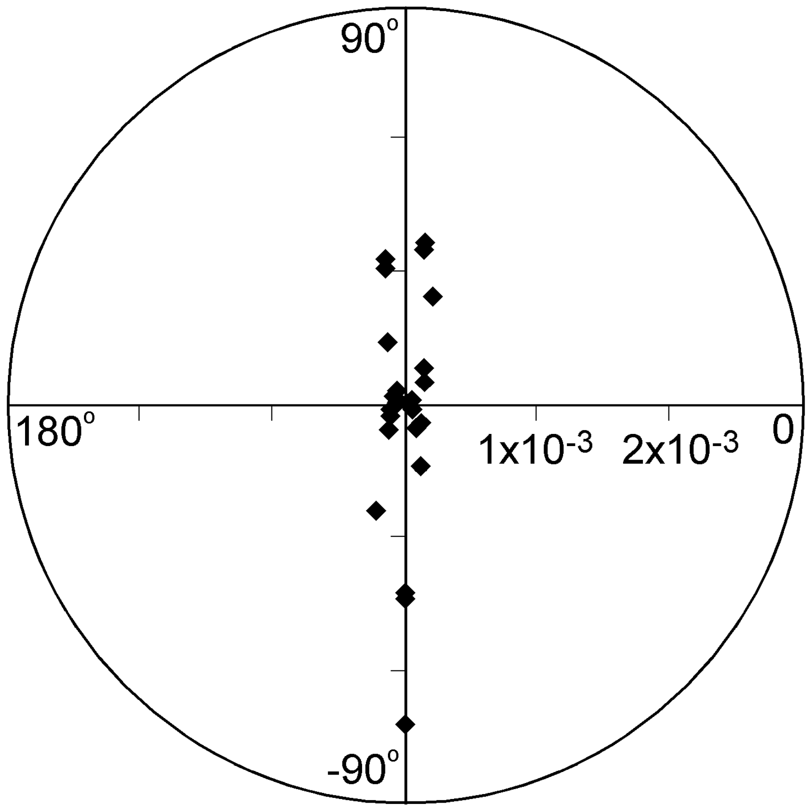
Test Development

Special Problems

- Part De-lidding
- In Vacuum Operation

Toshiba Angle Plot

Cross Section vs. Azimuthal Angle for a Toshiba 64Mb DRAM Using F at 48° (polar plot)



Summary

- SEE Effects Are an Important Issue for All Spacecraft
- Testing and Evaluation of the Impact of SEE Is a Complex Problem
  - Few problems with older spacecraft because of thorough testing
  - Likely to become more severe for newer technologies
- Section 514 Continually Evaluates SEE Effects
  - Direct Support to Many JPL Programs
  - Testing of Advance Microprocessors for REE
  - Evaluation of Advanced Devices under the NEPP Program